SHIVAJI UNIVERSITY, KOLHAPUR

B.Sc. Part-III Physics CBCS (Semester-V)

PHYSICS Paper-XII

DSE-E4 Digital and Analogue Circuits and Instrumentation

Unit –I 1.Digital Electronics

1. --------is a logic circuit with one or more input signals, but only one output signal.
   (A) Counter (B) Flip Flop
   (C) counter **(D) gate**
2. For ------- gate, output is high when any of the input is high.
   (A) AND (B) OR
   (C) NOR (D) NOT
3 ---------- gate is called as inverter.
   (A) OR (B) AND
   (C) **NOT** (D) NOR
4. Derived gates are ----------
   (A) OR, AND, NOT (B) **NOR, NAND, Ex-OR**
   (C) OR, NAND, NOT (D) NOR, AND, NOT
5. Basic or fundamental gates are ----------.
   (A) **OR, AND, NOT** (B) NOR, NAND, Ex-OR
   (C) OR, NAND, NOT (D) NOR, AND, NOT
6. NAND gate is also called as _____ gate.
   (A) unique (B) logic
   (C) **universal** (D) two input
5. The HIGH state in digital logic represents ----------
   (A**) +5 volt** (B) +12 volt
   (C) -5 volt (D) 0 volt
8. A binary 1 represent a ------- level and a binary 0 represent ------level.
   (A) low, high (B) **high, low**
   (C) high, high (D) Low, low
9. The input and output states of a gate are listed in a table called _____
   (A)data table (B)**truth table**
   (C) input-output data (D)input-output condition

10. For ------- gate, output is high when both the inputs are high.
    (A) 0R (B) **AND**
    (C) NAND (D) NOR
11. For Ex-OR gate when both the inputs are same output is -----.
    (A) **LOW** (B) HIGH
    (C) -5 VOLT (D) -1

12. The boolean equation for OR gate is ----------

(A) Y=A*B (B) Y=A-B

(C) Y=A.B (D) **Y=A+B**

13. Example of two input quad NAND gate is_____

(A) **IC 7400** (B) IC 7408

(C) IC 7402 (D)IC7486

14. IC 74XX series represents ------- family .

(A)**TTL** (B) RTL

(C) DTL (D) CMOS

15.----- is a two state circuit that can remain in either state indefinitely.

(A)**Flip-flop** (B) Gate

(C) Counter (D) Half adder

16. RS flip-flop is designed using ---------- gate.

(A) AND (B) **NAND**

(C) NOT (D) OR

17. --------- flip-flop is very versatile and is most widely used type of flip-flop.

(A) RS (B)**JK**

(C) D- type (D) clocked RS

18. Toggling more than once during a positive clock edge is called -----

(A**) race condition** (B) steady state

(C) unstable state (D) switching state

19. Memory blocks are designed using --------

(A) logic gates (B) counter

(C**) flip-flops** (D) half adders

20 --------- wave form is used as clock signal in flip flops.

(A) **square** (B)sine

(C) triangular (D)saw tooth

21. In RS flip flop when S=l and R=0 then flip flop is in ----- condition.

(A) **set** (B) reset

(C) race (D) toggle

22. Example of two input XOR gate is_____

(A) IC 7400 (B) IC 7408

(C) IC 7402 (**D)IC7486**

Unit I : 2. Amplifier

1. To draw d.c. equivalent circuit, reduce all---------- fo zero.

(A) ac sources (B) d.c. sources

(C)current sources (D)voltage source

1. _____ circuit increases the amplitude of weak input signal given to it.

(A)amplifier (B)scillator

(C) rectifier (D) transmitter

2. ---------- equivalent circuit, all capacitors are shorted.

(A) volatge (B) d.c

(C) current **(D) a.c.**

3. The relation between Vce and Ic represented by a straight line on output characteristic curve is known as a ----------

(A) frequency response (B) frequency curve

(C) load-line (D) amplifier line

4. The voltage gain of an amplifier is expressed in _____

(A)Volts (B) ampere

(C) decibel(dB) (D)bell

5. The purpose of d.c. conditions in a transistor is to ---------

(A) Reverse bias the emitter (B) Forward bias the collector

(C) Set up operating point (D) start its working

6. A CE amplifier is also called -------circuit.

(A) grounded emitter (B) grounded bias

(C) grounded collector (D) open collector

7. --------- equivalent circuit all capacitors are open circuited.

(A)a.c. **(B) d.c.**

(C) voltage (D) current

8. The phase difference between output and input signal in CE amplifier is _____-degree.

(A) 0 (B) 60

(C) 90 **(D)180**

9. --------source produces fluctuations in the transistor current and voltage .

(A) volatge source (B) d.c. source

(C)current source **(D) a .c. source**

10. ---------- on the output characteristics of a transistor circuit gives the values of Ic and Vce corresponding to zero signal.

(A)Straight line (B)a.c.load line

(C) d.c.load line (D)both (b) & (c)

11. In single stage CE amplifier_____ transistor is used.

(A)four (B) three

(C)two **(D) one**

12. The point of intersection of d.c. and a.c. load line is called _____

(A)Intersection point **(B) Quiescent operating point**

(C) dc point (D) a.c. point

13. The curve between voltage gain and signal frequency of an amplifier is known as — curve.

(A)band width **(B)frequency response**

(C) gain response (D)output

14. In a transistor

(a) Ie=Ic+Ib (b) Ie=Ic-Ib (c) Ic=Ie+Ib (d) Ib=Ic+Ie

15. The most commonly used transistor arrangement is ----------

(a) Common emitter (b) Common base

(c) Common collector (d) common source

3. Oscillator

1. --------- is an electronic circuit which converts d.c. energy info a.c. energy.

(A) Amplifier (B) **Oscillator**

(C) Op-amp (D) Flip-Flop

2. A circuit which produces electrical oscillations of any desired frequency is known as --------

(A) **Oscillatory circuit** (B) Amplifier circuit

(C) frequency generator (D) Invertor

3) Tank circuit produces ---------- oscillations.

(A)undamped (B) **damped**

(C) sinusoidal (D) any shape

4. For Barkhausen criteria for sustained oscillation A□□value must be ----------

(A) 0 (b) 2

(C) less than 1 (D)**1**

5. In phase-shift oscillator, the phase shift in each RC network is ----------

(A) 90^0 (B)120^0

(C) 60^0 (D) 45^0

6. In phase-shift oscillator, the feedback factor beta is ---------

(A) 1/20 (B) **1/29** (C)1/25 (D) 1/30

7. In --------- oscillator, two capacitors are placed across a common inductor.

(A)Phase-shift (B) **Collpit's**

(C) Wein-bridge (D) Hartley

8 Tank circuit provides phase shift of ----------

(A) 45^0 (B) 60^0

(C) 360^0 **(D) 180^0**

9. Oscillator is an electronic circuit which converts ----- energy into a.c. energy.

(A) a.c . (B) **d.c.**

(C) solar (D) wind

10. An oscillator circuit uses -------- feedback.

(A) **positive** (B) negative

(C) current (D) positive and negative

11. In phase-shift oscillator, the frequency determining elements are --------

(A) R (B) C

(C) **R and C** (D) L and C

12. In the Colpitt's oscillator, the frequency determining elements are --------

(A) R (B) C

(C) R and C (D) **L and C**

13. Expression for frequency of phase shift oscillator is ----------

$(A) f_o = \frac{1}{2\pi RC}$ **(B)** $f_o = \frac{1}{2\pi\pi R\sqrt{6}}$

$(C) f_o = \frac{1}{2\pi\sqrt{RC}}$ $(D) f_o = \frac{1}{2\pi\sqrt{LC}}$

14. Expression for frequency of Colpitt's oscillator is ----------

$a) f_o = \frac{1}{2\pi RC\sqrt{6}}$ $b) f_o = \frac{1}{2\pi RC}$ **c)** $f_o = \frac{1}{2\pi\sqrt{LC}}$ $d) f_o = 2\pi\sqrt{LC}$

15. In Hartley oscillator, frequency of the oscillations fo is -----

$a) f_o = \frac{1}{2\pi RC\sqrt{6}}$ $b) f_o = \frac{1}{2\pi RC}$ **c)** $f_o = \frac{1}{2\pi\sqrt{LC}}$ $d) f_o = 2\pi\sqrt{LC}$

15. The equivalent capacitor in Colpitt's or crystal oscillator is given by ----------

(A) $C = \frac{C1.C2}{C1 + C2}$ $(B) C = \frac{C1.C2}{C1 - C2}$

$(C) C = \frac{C1 - C2}{C1 + C2}$ $(D) C = \frac{C1 + C2}{C1 - C2}$

16. The crystal oscillator is used to produce --------- frequencies.

(A) moderate (B) low

(C) **High** (D)very low

17. Oscillator circuits are useful in ---------

(A) amplifier (B**) transmitter**

(C) receiver (D) logic gates

18. The condition A=1 is known as ----------criterion.

(A) Collpitt's (B) Hartley

(C) Newton's (D) **Barkhausen**

Unit-II 1.CRO

1. A CRO is used to measure ----------

(A) voltage (B)frequency

(C)phase **(C) all A,B,C**

2. The most accurate device for measuring voltage is _____

(A) voltmeter (B)multirneter

(C) C.R.O. (D) milivoltmeter

3. If the negative potential on the control grid of CRT is increased, the intensity of spot is _____

(A) increased (B)**decreased**

(C)remains the same (D)varies

4. The gain control of the vertical amplifier is calibrated in terms of ----------

(A) current (B)voltage

(C)Potential (D)**deflection sensitivity**

5. ---------- is used to obtain required potentials for various electrodes in CRT.

(A) **potential divider** (B) resistor bias

(C)capacitor bias (D) d.c.bias

6. ----------plates are mounted in the vertical plane.

(A) vertical deflection (B)**horizontal deflection**

(C)electron gun (D) control grid

7. CRT stands for ----------

(A) Cathode Ray light Tube (B) Caloric Radiation Tube

(C)**Cathode Ray Tube** (D) Cathode Ray Telescope

8 The gain of the vertical amplifier can be controlled by the ---------

(A) gain controller (B) **input attenuator**

(C) voltage divider network (D)RC network

9. To remove the electrons from the screen, the side walls of CR are coated with ---------- particles.

(A) **carbon** (B) phosphor

(C) zinc (D) calcium

10 ---------- plates are mounted horizontally on the tube.

(A) **vertical deflection** (B)) horizontal deflection

(B) electrical (D) deflecting

11. Inner wall of CRT is coated with conducting material called ----------

(A) attenuator (B) conducting Chanel

(C) **aquadag** (D) carbon chanel

12 ------- is an electronic device which is capable to give visual indication of a signal waveform.

(A) **C.R.O.** (B) CRT

(C) VTVM (D) multimeter

13 CRO stands for ----------

(A) **Cathode Ray Oscilloscope** (B) Cathode Rays Oscillograph

(C) Cathode Ray Oscillator (D) Cathode Rays

14 Arrangement of electrodes which produce a focused beam of electrons on screen is called the ---------

(A) electron tube (B) **electron gun**

(C) electronic gun (D) electron control

15 CRO is basically a ------- plotter.

(A) **X-Y plotter** (B)X-plotter

(C) Y-plotter (D)X-Z plotter

16 By varying the negative potential of --------- the intensity of the spot on the screen is controlled.

(A)anode (B) cathode

(C) **control grid** (D) plates

17 When both horizontal and vertical plates are subjected to ac voltages,------figures are displayed on the screen.

(A)geometric (B)beautiful

(C) **Lissajous** (D)interesting

18. To start the horizontal sweep at a specific instant _ _ _ _ _ _ _circuit is provided.

(A) **time base** (B) voltage divider

(C) amplifier (D) square wave

19. When ---------- voltage is given to X-plates, the spot moves to the right on the screen to reach the maximum distance.

(A) **saw tooth** (B) sine wave

(C) square wave (D) d.c.

20) ----------produces a narrow beam of electrons which can be focused on the screen.

(A) electron tube (B) **electron gun**

(C) electronic gun (D) electron control

21. Any unknown voltage to be measured using C.R.O. is applied to --------- input of C.R.O.

(A) X (B**) Y** (C) Z (D) X-Y

2. Operational Amplifier

1) Differential amplifier can be used as a building block for --------

a) Operational amplifier b) negative feedback amplifier

c) positive feedback amplifier d) feedback amplifier

2) One of the input of differential amplifier is called inverting input because its output is ----------

a) **180^0out of phase with input** b) in phase with input

c) in phase as well as out of phase with inputs d) 90^0out of phase with input

3) Widely used differential amplifier is ----------

a) double ended input and output **b) double ended input and single ended output**

c) single ended input and double ended output d) single ended input and output

4) In case of differential amplifier, input is applied between ---------

a) emitters of two transistors b) collectors of two transistors

c) bases of two transistors d) emitters of four transistors

5) Common mode rejection ratio = ------

a) $\frac{R_E}{r'_e}$ b) $\frac{R_C}{r'_e}$ c) $\frac{R_B}{r'_e}$ d) $\frac{R}{r'_e}$

6) Input offset voltage is -------

a) the average of both input currents b) the difference of the input bias currents

c) equal to the difference in V_{BE} values of input transistors

d) equal to the difference in V_{CE} values of input transistors

7) Ideal op- amp has ----------input impedance

a) zero **b) infinite** c) finite d) large

8) Op amp amplifies -------

a) dc signals b) ac signals

c) both ac & dc signals d) neither ac nor dc signals

9) The closed loop gain of non-inverting amplifier is Acl = -------

a) $\frac{R_f}{R_{in}}$ b) $-\frac{R_f}{R_{in}}$ **c)** $1+\frac{R_f}{R_{in}}$ d) $1-\frac{R_f}{R_{in}}$

10) If the op-amp subtractor circuit has $R_f = 4R_{in}$ and V_1 = 3mV and V_2 = 1 mV, then its output is ----

a) 4 mV b) 1 mV **c) 0.25 mV** d) 2.5 mV

11) Op-amp as an inverting amplifier can be used as a integrator by connecting a ---------- in feedback path.

a) resistance **b) capacitor** c) inductance d) diode

12. IC _____ is widely used as an op-amp *

(A) 741 b)742 C)743 d)7401

13. Differential amplifiers uses ---------- stages of amplifiers.

a) four balanced **b) two balanced**

c) three balanced d) two unbalanced

14. How many modes of operation of a differential amplifier?

a) three b) two c) five **d) four**

15. In case of double ended input and single ended output differential amplifier output is taken -----

a) between emitters of two transistors b) between collectors of two transistors

c) between bases of two transistors **d) between the collector of a transistor and ground.**

16. Gain of differential amplifier is ----------

a) very small **b) very high** c) zero d) infinite

17. Common mode rejection ratio is the ratio of----

a) differential voltage gain to common mode voltage gain

b) common mode voltage gain to differential voltage gain

c) differential voltage gain to common mode current gain

d) differential current gain to common mode voltage gain

18. Input offset current is -------

a) the average of both input currents **b) the difference of the input bias currents**

c) equal to the difference in V_{BE} values of input transistors

d) equal to the difference in V_{CE} values of input transistors

19. An ideal op-amp- has --------

a) zero input impedance b) finite input impedance

c) infinite input impedance d) infinite output impedance

20. The gain of operational amplifier with feedback is called------

a) closed loop gain b) infinite loop gain

c) moderate loop gain d) open loop gain

21. The closed loop gain of inverting amplifier is Acl = -------

a) $\frac{R_f}{R_{in}}$ **b)** $-\frac{R_f}{R_{in}}$ c) $1+\frac{R_f}{R_{in}}$ d) $1-\frac{R_f}{R_{in}}$

22. If the op-amp subtractor circuit has $2R_f = R_{in}$ and V_1 = 3mV and V_2 = 1 mV, then its output is ----

a) 2 mV b) 1 mV c) 0.5 mV d) 2.5 mV

23. Op-amp as an inverting amplifier can be used as an ----------by connecting a capacitor in feedback path in place of feedback resistance.

a) comparator b) differentiator

c) adder/subtractor **d) integrator**

24. How many transistors are used in the differential amplifier?

a) only one **b) only two** c) one or two d) more than two

25. One of the input of differential amplifier is called non-inverting input because its output is ----------

a) 180^0out of phase with input **b) in phase with input**

c) in phase as well as out of phase with inputs d) 90^0out of phase with input

26.In case of double ended output differential amplifier, output is taken across ---------

a) emitters of two transistors **b) collectors of two transistors**

c) bases of two transistors d) emitters of four transistors

27.Differential amplifiers has ---------

a) lower i/p impedance and higher o/p impedance

b) very high o/p impedance and low i/p impedance

c) higher i/p impedance and lower o/p impedance

d) higher i/p impedance and higher o/p impedance

28. CMRR stands for ----------

a) Common Mode Referential Ratio b) Common Mode Reference Ratio

c) Common Mode Rejection Ratio d) Commercial Mode Reference Ratio

29. Input bias current is -------

a) the average of both input currents

b) the difference of the input bias currents

c) equal to the difference in V_{BE} values of input transistors

d) equal to the difference in V_{CE} values of input transistors

30. For ideal op-amp open loop gain is -------

a) zero b) greater than one c) less than one **d) infinite**

31. The gain of operational amplifier without negative feedback is called------

a) closed loop gain b) infinite loop gain

c) moderate loop gain **d) open loop gain**

32. If the op-amp subtractor circuit has $R_f=2R_{in}$ and V_1 = 3mV and V_2 = 1 mV, then its output is ----

a) 2 mV b) 1 mV **c) 0.5 mV** d) 2.5 mV

33. Op-amp as an inverting amplifier can be used as an ----------by connecting a capacitor in feedback path in place of feedback resistance.

a) comparator b) differentiator

c) adder/subtractor **d) none of these**

34.) Op-amp as an inverting amplifier can be used as a ----------by connecting a capacitor in input path in place of resistance.

a) comparator **b) differentiator**

c) adder/subtractor d) integrator

35. The frequency at which the voltage gain equals 1 is called as----------

(A) Unit gain frequency (B) average frequency
(C) standard frequency (D) stable frequency

36. An ideal Op-Amp has ..... bandwidth

(A)infinite (B)finite (C)limited (D) zero

Topic: Timer IC555

1. IC 555 consists of ---------- comparator

(a) two (b) three (c) four (d) five

2. --------- R-S flip-flops are present in IC-555.

(a) four (b) three **(c) two** d) one

3. ---------- is not a terminal of IC-555 .

(a) threshold (b) trigger **(C) gate** (d) reset

4. In IC 555, ----- pin is internally connected to the collector of the Transistor.

a) control (b) trigger (c) discharge **(d) threshold**

5. Basic version of IC-555 in package ..... pins.

a) 8 (b) 10 (c) 12 (d) 14

6. Astable multivibrator is also called as ----------

(A) one shot (B) monostable (C) bistable **(D) free running**

7. Voltage at trigger pin of IC555 is ----------

(a) 2VCC (b) Vcc **(c) 1/3Vcc** (d) 2/3Vcc

8. Voltage at threshold pin of IC555 is ----------

(a) 2VCC (b) Vcc (c) 1/3Vcc **(d) 2/3Vcc**

9. When timer is reset then its output is .....

(a) zero (b) high (d) 2Vcc (d) V cc

10. --------- multivibrator has no stable state/states.

(a) astable (b)bistable (c) mono (d) flipflop

10. Monostable multivibrator has ..... stable state and one quasistable state.

(a) 0 **(b) 1** (c) 2 (d) 3

11. Number of stable states in bistable multivibrator is .....

(a) zero (b) 1 (c) infinite **(d) 2**

12. The output state of IC-555 timer cannot be changed by changing voltage at ..... terminal.

(a) discharge (b) trigger (c) threshold (d) reset

13. Pulse width of monostable multivibrator depends on values of--------

(a)RC (b) (R1 + 2R2) C (b) (R1 + R) RC (d) (2R1 + R2)

14. Frequency of astable multivibrator depends on .....

(a)only R2 (b) only R1 (c) only C **(d) R1, R2 and C**

15. Duty cycle in astable multivibrator varies between ....

(a) 0 to 0. 5 (b) 0.5 to 1 (c) 1 to 1.5 (d) 0 to 1.5

16. -------- multivibrators is used as a memory cell.

(a) bistable (b) monostable (c) astable (d) free running

17. ---------- requires no trigger input.

(a) bistable (b) monostable **(c) astable** (d) free running

18. Pulse width of monostable multivibrator depends on values of--------

(a)RC (b) (R1 + 2R2) C (b) (R1 + R) RC (d) (2R1 + R2)

19 The time period of Timer 555 astable multivibrator is given by ----------

(A) $T=0.33R_AC$ (B) $T=1.1(R_A+2R_B).C$ (C) $T= T=0.693(R_A+2R_B).C$

(D) $T= (R_A+2R_B).C$

20. The time period of Timer 555 monostable multivibrator is given by ---------

(A) T=0.33RC (B) T=1.1RC (C) T=RC (D) T=0.6RC

21. Frequency of astable multivibrator depends on .....

(a)only R2 (b) only R1 (c) only C **(d) R1, R2 and C**

22. Duty cycle in astable multivibrator varies between ....

(a) 0 to 0. 5 (b) 0.5 to 1 (c) 1 to 1.5 (d) 0 to 1.5

========== VVK==========